NATIONAL INSTITUTE OF TECHNOLOGY SIKKIM

in association with

NOVEL INTEGRATED ELECTRONICS LABS (NINE LABS), IIT Guwahati

Organizing a

Workshop on "VLSI Design Using Open Source Tools"

Sponsored by "Ministry of Electronics and Information Technology (MeitY)"

OUTCOME

The workshop on Opensource EDA Design tool, OpenROAD, is organized to bring together researchers, developers, and users to discuss advancements, share knowledge, and collaborate on open-source tools for chip design. After completion of this workshop, participants would be able to design digital circuits through VLSI backend flow.

TENTATIVE SPEAKERS

PRINCIPAL INVESTIGATOR

Prof. Gaurav Trivedi
Professor, Department of EEE
IITG

KEYNOTE SPEAKER

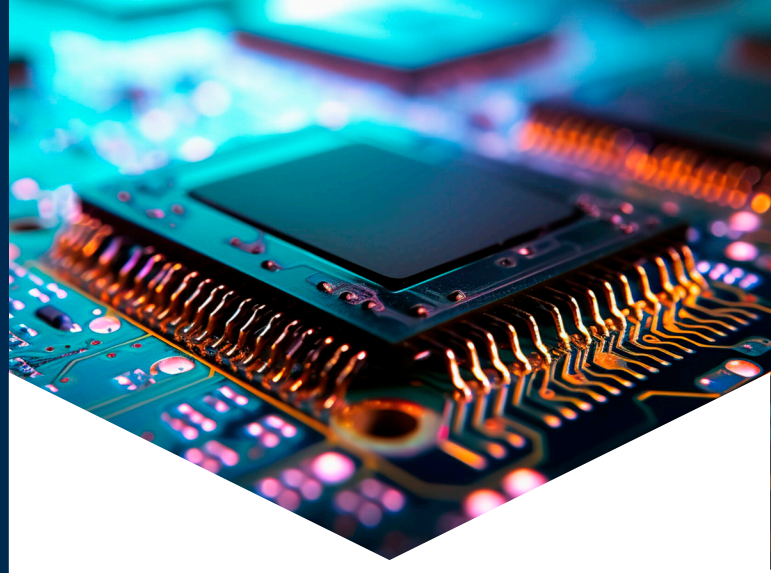
Ms. Indira Iyer Almeida
Program Director,
The OpenROAD Initiative

INVITED SPEAKER

Mr. Gadiparthi Naveen
(Chipware Technologies)

DETAILS

10TH – 14TH MAR 2026
MULTI PURPOSE HALL
NATIONAL INSTITUTE OF TECHNOLOGY SIKKIM
SIKKIM – 737139,INDIA



OBJECTIVE

The objective of this workshop is to train the participants with VLSI design backend flow through the open-source VLSI design tool "OpenROAD". After successful completion of this workshop, the participants would be able to run the RTL synthesis to GDS-II flow for their own design.

CONTACT

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CONTENTS

- **Introduction to VLSI Backend Flow**
  - Stages and Sign-off Checks Overview
  - OpenROAD Design Flow
  - Detailed VLSI Backend Flow
  - RTL Synthesis
  - Floorplanning
  - Placement
  - Static Timing Analysis
  - Clock Tree Synthesis
  - Routing
  - GUI
  - OpenROAD for PPA
- **Hands-on**
  - Installation of the OpenROAD Tool.
  - Input files
  - RTL synthesis
  - Sanity Checks
  - Floorplan and Placement
  - Post-placement Timing Analysis
  - Clock Tree Synthesis (CTS)
  - Post-CTS Timing Analysis
  - Routing and DRC/LVS Check.

WHO CAN APPLY?

UG/PG students/Research Scholars of ECE/EEE/Technical Institutions

HOW TO APPLY?

Reg. Link:
https://forms.gle/9gEiCFATxRZd7C1s8

Workshop Mode: Offline
Workshop Duration: 5 days
Accommodation would be made available only for the offline participants on request

TRAINING PARTNER

Chipware Technologies

ORGANIZING COMMITTEE

Prof. Mahesh Chandra Govil
(Patron)
Dr. Jeetendra Singh
(Convener)
Dr. Hemant Kumar Kathania
(Convener)
Dr. Sanjay Kumar Jana
(Convener)

VOLUNTEERS

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