Topics to be covered

- RTL design, simulation & synthesis (Vivado)
- FPGA implementation & hardware debugging
- Industry-standard RTL-to-GDSII ASIC flow
- Logic synthesis & STA
- Floorplanning, Placement & Routing
- Physical verification (DRC/LVS/PEX)
- GDS-II generation & sign-off overview

About the Institute

National Institute of Technology Sikkim (NIT Sikkim), established in 2010 under the Government of India's 11th Five-Year Plan, is one of the country's prominent institutes of higher education. Nestled in the serene Himalayan region, it offers undergraduate, postgraduate, and doctoral programs across engineering, technology, and applied sciences. The institute is dedicated to delivering quality education while promoting innovation and research. Over the years, NIT Sikkim has built a strong academic reputation, with its students consistently earning placements in leading national and international companies

About the Department

The Department of Electronics and Communication Engineering (ECE) at NIT Sikkim, established in 2010, offers B.Tech, M.Tech, and Ph.D. programs with strong focus areas such as VLSI design, communication systems, signal processing, microwave engineering, and semiconductor technologies. Supported by modern labs and a dedicated faculty team, the department blends strong theoretical foundations with practical exposure. Through internships, industry interaction, expert lectures, and activities by its technical club *Anuvrat*, it fosters holistic student development and prepares graduates for advanced careers in industry and research.

About Sikkim

Sikkim, a small but picturesque state nestled in the northeastern part of India, is known for its breathtaking landscapes, rich biodiversity, and vibrant cultural heritage. Bordered by Bhutan, Tibet, and Nepal, it is home to the majestic Kanchenjunga, the third-highest mountain in the world. Sikkim boasts a unique blend of ethnic communities, including Lepchas, Bhutias, and Nepalese, each contributing to its diverse traditions and festivals. The state is also noted for its environmental consciousness, being the first fully organic state in India.

Objectives of the event

- Introduce learners to modern digital design flows encompassing both reconfigurable FPGA platforms and full-custom ASIC development pipelines.
- Enable hands-on expertise in Xilinx Vivado for RTL design, simulation, synthesis, implementation, and hardware debugging.
- Train students and researchers in the industry-standard RTL-to-GDSII ASIC design flow.
- Provide exposure to key backend stages including synthesis, static timing analysis, floor-planning, placement & routing, physical verification (DRC/LVS/PEX), and GDS-II file generation.
- Promote research and innovation in IC design among UG/PG students, researchers, and faculty of the North East Region.
- Prepare the next generation of skilled VLSI engineers to contribute to the India Semiconductor Mission and strengthen India's chip-design ecosystem

राष्ट्रीय प्रौद्योगिकी संस्थान, सिक्किम

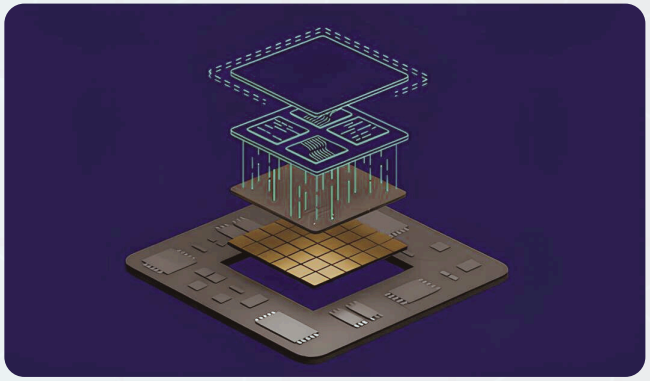
National Institute of Technology Sikkim

(An Institute of National Importance, Ministry of Education, Govt. of India)

5 days Advanced workshop on "Hardware Implementation of Digital Systems & RTL-GDSII ASIC Flow"

"Building India's Silicon Future"

(13th to 17th April, 2026)



Organized by

Department of Electronics and Communication Engineering

National Institute Of Technology Sikkim
Barfung Block , Ravangla,
South Sikkim-737139(India)

(An autonomous Institute under the aegis of the Ministry of Education, Govt. of India)
website: https://nitsikkim.ac.in/

About the Workshop

This workshop provides a comprehensive introduction to modern digital VLSI design flows, covering both reconfigurable FPGA platforms and industry-standard ASIC development pipelines. Participants will gain hands-on experience in RTL design, simulation, synthesis, and FPGA implementation using Xilinx Vivado, along with practical exposure to hardware debugging. The program also introduces the complete RTL-to-GDSII ASIC flow, including logic synthesis, static timing analysis, floorplanning, placement and routing, physical verification (DRC/LVS/PEX), and GDS-II generation. Designed to promote research-driven learning and skill development, the workshop aims to prepare students, researchers, and faculty to contribute effectively to advanced IC design and India's growing semiconductor ecosystem.

Other instructions

This workshop will be conducted in **offline mode**.

- Shared accommodation and meals will be provided by NIT Sikkim for all participants.
- NIT Sikkim, Ravangla, is located at an altitude of 2100 meters and experiences cold weather throughout the year. Participants are advised to carry adequate warm clothing.
- For any queries, participants are encouraged to contact the workshop conveners.

Resource persons

Eminent acdemicians from IITs & NITs, along with experienced professionals from the semiconductor and VLSI industry

Who can attend

The faculty members, Research scholars & PG Scholars of the technical institutions and Industry Personnel

Patron

Prof. Mahesh Chandra Govil,
Director, NIT Sikkim.

Chair Person

Dr. Sanjay Kumar Jana,
Associate Professor, ECE.
NIT Sikkim.

Convener

Dr. Jeetendra Singh
Assistant Professor, ECE.
NIT Sikkim.

Coordinators

Dr. Hemant Kumar Kathania
Assistant Professor & HoD, ECE.
NIT Sikkim.

Dr. Abhishek Rajan
Assistant Professor, EEE.
NIT Sikkim.

Organizing committee

Dr. Reshmi Dhara, Assistant Professor, ECE
Dr. Varun Gupta, Assistant Professor, ECE
Dr. Vishal Vishnoi, Assistant Professor, ECE
Dr. Sudipta Das, Temporary Faculty, ECE
Dr. Jayshree, Temporary Faculty, ECE
Mr. Amit Tamang
Mr. Sidharth Pradhan

Registration and general information

Interested candidates are required to register for the workshop using the Google Form link or the QR code provided below

CLICK HERE FOR REGISTRATION

REGISTRATION FEE: Rs. 500/- Only

The number of participants is limited and will be selected based on a first-come, first-served basis, and a prerequisite.

Last date of registration: 05th April, 2026

Participants can complete their payment through the following details:

Account Holder's Name : DIRECTOR NIT SIKKIM
Account Number : 31996269106
Bank Name : State Bank of India
Branch & IFSC : Ravangla, SBIN0007218

For any clarification, the workshop convener can be contacted.

Contact us

Convener: Dr. Jeetendra Singh
Email: jeetendra@nitsikkim.ac.in
Mobile: +91-9046227909