Curriculum and Syllabus of M.Tech Degree Programme in Microelectronics and VLSI Design

Effective from Admission year 2019 - 20 onwards

Department of Electronics & Communication Engineering

National Institute of Technology Sikkim

South Sikkim 737 139

Syllabus: Core Subject

Semester 1

Subject Code	Subject Name	L-T-P	Credit
EC 21103	Analog MOS Integrated Circuits Design	3-0-0	3

Module 1 (8 hours)

Introduction to Analog Design. Basic MOS device physics. MOSFET I-V characteristics. threshold voltage, current, 2^{nd} order effects: Channel length modulation, body bias effect and short channel effects, MOS switch, MOSFET capacitances, MOS small Signal Model.

Module 2 (10 hours)

Single – stage amplifiers: CS stage with registive load, CS stage with diode-connected load, CS stage with triode load, CS stage with source degeration. Common Gate stage, Cascode stage.

Module 3 (10 hours)

Differential Amplifier: single-ended and differential operation. Basic differential Pair: qualitative Analysis, quantative Analysis. Common Mode Response. Differential Pair with MOS loads. Gilbert Cell. Passive and active current mirror.

Module 4 (12 hours)

Frequency Response of Amplifiers. Miller effect, CS, CG, CD, Cascode stage, Differential Pair. Noise: Statistical Characteristics of Noise. Types of Noise. Representation of Noise in circuits. Feed Back, Design of One stage and two stage Op-Amps. PLL

Text Book: 1. Behzad Razavi " Design of Analog CMOS Integrated Circuits" Mc Graw Hill Education.

References:

1. Phillip E. Allen, Douglas R Holberg, South Asia Edition, Oxford University Press.
2. Gray Hurtst lewis and Meyer "Analysis and Design of analog Integrated Circuits" Wiley 5th student edition.

Subject Code	Subject Name	L-T-P	Credit
EC21102	Computational Mathematics	3-0-0	3

Module I

Basic definitions, Degree of vertices, Complement of a graph. Self-complementary graph, some eccentricity properties of graphs. Tree, spanning tree. Directed graphs standard definitions; strongly, weakly, unilaterally connected digraphs, deadlock communication network. Matrix representation of graph and digraphs. Some properties (proof not expected).

Module II

Eulerian graphs and standard results relating to characterization. Hamiltonian graph-standard theorems (Dirac theorem, Chavathal theorem, closure of graph).Non Hamiltonian graph with maximum number of edges. Self-centered graphs and related simple theorems. Chromatic number; Vertex and edge (only properties and examples)-application to colouring. Planar graphs, Euler's formula, maximum number of edges in a planar graph. Five colour theorem.

Module III

DFS-BFS algorithm, shortest path algorithm, min-spanning tree and max-spanning tree algorithm, planarity algorithm. Matching theory, maximal matching and algorithms for maximal matching. Perfect matching (only properties and applications to regular graphs).

Flows in graphs, Ranking of participants in tournaments, simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs. PERT-CPM. Complexity of algorithms; P-NP- NPC-NP hard problems and examples.

Module IV

Linear- Integer Linear programming, Conversion of TSP, maxflow, Knapsack scheduling, shortest path problems for Linear programming types - branch bound method to solve Knapsack problems- critical path and linear programming conversion- Floor shop scheduling problem- Personal assignment problem.

Dynamic programming- TSP- compartment problems- Best investment problems.

Text Books

1. C.Papadimitriou&K.Steiglitz, "Combinatorial Optimization", Prentice Hall, 1982.
2. H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.
3. J.A.Bondy&U.S.R.Murthy, "Graph Theory with Applications", Macmillan, London, 1976,

EBook, Freely Downloadable.

4. Cormen, Leiserson, Rivest& Stein, “Introduction to Algorithms”,2nd Edition, McGraw-Hill, 2001.

Reference Book

1. B.Korte&J.Vygen, “Combinatorial Optimization”, Springer-Verlag, 2000.

Subject Code	Subject Name	L-T-P	Credit
	Elective I	3-0-0	3

Subject Code	Subject Name	L-T-P	Credit
	Elective II	3-0-0	3

Subject Code	Subject Name	L-T-P	Credit
	Elective III	3-0-0	3

Practical subjects

Subject Code	Subject Name	L-T-P	Credit
EC21201	Analog MOS Integrated Circuits Lab	0-0-3	2

Subject Code	Subject Name	L-T-P	Credit
	Laboratory I	0-0-4	2

Subject Code	Subject Name	L-T-P	Credit
	Laboratory II	0-0-4	2

Subject Code	Subject Name	L-T-P	Credit
	Laboratory III	0-0-3	2

Semester II

Subject Code	Subject Name	L-T-P	Credit
EC 22101	Device Modeling	3-0-0	3

Module 1 (13 hours)

Semiconductor surfaces, Ideal MOS structure, MOS device in thermal equilibrium, Non-Ideal MOS: work function differences, charges in oxide, interface states, band diagram of non ideal MOS, flatband voltage, electrostatics of a MOS (charge based calculations), calculating various charges across the MOSC, threshold voltage, MOS as a capacitor (2 terminal device), Three terminal MOS, effect on threshold voltage.

Module 2 (10 hours)

MOSFET (Enhancement and Depletion MOSFETs), mobility, on current characteristics, off current characteristics, sub threhsold swing, effect of interface states on sub threshold swing, drain conductance and transconductance, effect of source bias and body bias on threshold voltage and device operation.

Module 3 (6 hours)

Scaling, Short channel and narrow channel effects- High field effects.

Module 4 (5 hours)

MOS transistor in dynamic operation, Large signal Modeling, small signal model for low, medium and high frequencies.

Module 5 (8 hours)

SOI concept, PD SOI, FD SOI and their characteristics, threshold voltage of a SOI MOSFET, Multi-gate SOI MOSFETs, Alternate MOS structures.

References:

1. E.H. Nicollian, J. R. Brews, Metal Oxide Semiconductor - Physics and Technology, John Wiley and Sons.

2. Nandita Das Guptha, Amitava Das Guptha, Semiconductor Devices Modeling and Technology, Prentice Hall India

3. Jean- Pierrie Colinge, Silicon-on-insulator Technology: Materials to VLSI, Kluwer Academic publishers group.

4. Yannis Tsividis, Operation and Modeling of the MOS transistor, Oxford University Press.

5. M.S.Tyagi, Introduction to Semiconductor materials and Devices, John Wiley & Sons, ISBN: 9971-51-316-1.

Subject Code	Subject Name	L-T-P	Credit
EC 22102	Testing and Verification of VLSI Circuits	3-0-0	3

Module 1

Fault models, Combinational logic and fault simulation, Test generation for Combinational Circuits. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation.

Module 2

Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

Module 3

Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause-effect diagnosis, Effect-cause diagnosis.

Module 4

Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing.

Module 5

Pattern Generators, Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

Text Books

1. N. Jha& S.D. Gupta, “Testing of Digital Systems”, Cambridge, 2003.
2. W. W. Wen, “VLSI Test Principles and Architectures Design for Testability”, Morgan Kaufmann Publishers. 2006.

Reference Books

1. Michael L. Bushnell &Vishwani D. Agrawal,” Essentials of Electronic Testing for Digital, memory & Mixed signal VLSI Circuits”, Kluwar Academic Publishers. 2000.
2. P. K. Lala,” Digital circuit Testing and Testability”, Academic Press. 1997.

Subject Code	Subject Name	L-T-P	Credit
	Elective IV	3-0-0	3

Subject Code	Subject Name	L-T-P	Credit
	Elective V	3-0-0	3

Subject Code	Subject Name	L-T-P	Credit
	Elective VI	3-0-0	3

Practical Subjects

Subject Code	Subject Name	L-T-P	Credit
EC22201	VLSI System Design Lab	0-0-4	2

Subject Code	Subject Name	L-T-P	Credit
EC22202	Advanced MOS Integrated Circuits Lab	0-0-4	2

Subject Code	Subject Name	L-T-P	Credit
	Laboratory III	0-0-4	2

Subject Code	Subject Name	L-T-P	Credit
	Laboratory IV	0-0-4	2

Semester III

Subject Code	Subject Name	L-T-P	Credit
EC 23101	Literature Review and Report Writing	0-0-2	4

Subject Code	Subject Name	L-T-P	Credit
EC 23201	Dissertation related Tools and Technologies	0-0-2	3

Subject Code	Subject Name	L-T-P	Credit
EC 23202	Dissertation Part-I	-	6

Semester IV

Subject Code	Subject Name	L-T-P	Credit
EC 24201	Dissertation Part-II	-	16