List of Electives			
EC2*111	Compound Semiconductors: Properties & Applications	3-0-0	3
EC2*112	MEMS and Microsystems and NEMS	3-0-0	3
EC2*113	Formal Verification of VLSI Circuits	3-0-0	3
EC2*114	Artificial Intelligence	3-0-0	3
EC2*115	Semiconductor Power Devices	3-0-0	3
EC2*116	Nanoelectronics	3-0-0	3
EC2*117	Low Power CMOS VLSI design	3-0-0	3
EC2*118	Mixed Signal RF IC design	3-0-0	3
EC2*119	CMOS RF circuit design	3-0-0	3
EC2*120	III-V semiconductors and High Speed electronic Devices	3-0-0	3
EC2*121	Biomedical Instrumentation	3-0-0	3
EC2*122	Advanced communication systems	3-0-0	3
EC2*123	Computer Architecture	3-0-0	3
EC2*124	VLSI Signal Processing	3-0-0	3
EC2*125	Semiconductor Materials and Device characterization	3-0-0	3
EC2*126	VLSI Technology and Processing	3-0-0	3
EC2*127	Introduction to VLSI Design	3-0-0	3
EC2*128	Analytical Techniques for VLSI	3-0-0	3
EC2*129	Signal Processing Technique	3-0-0	3
EC2*130	Embedded System	3-0-0	3
EC2*131	Internet of Things	3-0-0	3
EC2*132	Modeling of Digital Systems	3-0-0	3
EC2*133	Research Methodology	3-0-0	3

* The semester number in which the subject is offered.

Subject Code	Subject Name	L-T-P	Credit
EC2*111	Compound Semiconductors: Properties & Applications	**3-0-0**	**3**

Module 1 (6 hours)

Important parameters governing the high speed performance of devices and circuits: Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature; important parameters governing the high power performance of devices and circuits: Break down voltage, resistances, device geometries, doping concentration and temperature.

Module 2 (16 hours)

Materials properties: Merits of III –V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs, SiC, GaN etc.), different SiC structures, silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices, outline of the crystal structure, dopants and electrical properties such as carrier mobility, velocity versus electric field characteristics of these materials, electric field characteristics of materials and device processing techniques, Band diagrams, homo and hetro junctions, electrostatic calculations, Band gap engineering, doping, Material and device process technique with these III-V and IV – IV semiconductors.

Module 3 (8 hours)

Metal semiconductor contacts and Metal Insulator Semiconductor and MOS devices: Native oxides of Compound semiconductors for MOS devices and the interface state density related issues. Metal semiconductor contacts, Schottky barrier diode, Metal semiconductor Field Effect Transistors (MESFETs): Pinch off voltage and threshold voltage of MESFETs. D.C. characteristics and analysis of drain current. Velocity overshoot effects and the related advantages of GaAs, InP and GaN based devices for high speed operation. Sub threshold characteristics, short channel effects and the performance of scaled down devices.

Module 4 (12 hours)

High Electron Mobility Transistors (HEMT): Hetero-junction devices. The generic Modulation Doped FET(MODFET) structure for high electron mobility realization. Principle of operation and the unique features of HEMT, InGaAs/InP HEMT structures: Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high speed applications. GaAs and InP based HBT device structure and the surface passivation for stable high gain high frequency performance. SiGe HBTs and the concept of strained layer devices; High Frequency resonant –tunneling devices, Resonant-tunneling hot electron transistors

References:

1. C.Y. Chang, F. Kai, GaAs High-Speed Devices: Physics, Technology and Circuit Applications, Wiley & Sons.

2. Cheng T. Wang, Ed., Introduction to Semiconductor Technology: GaAs and Related Compounds, John Wiley & Sons.

3. David K. Ferry, Ed., Gallium Arsenide Technology, Howard W. Sams & Co., 1985

4. Avishay Katz, Indium Phosphide and Related materials: Processing, Technology and Devices, Artech House, 1992.
5. S.M. Sze, High Speed Semiconductor Devices, Wiley (1990) ISBN 0-471-62307-5
6. Ralph E. Williams, Modern GaAs Processing Methods, Artech (1990), ISBN 0-89006-343-5,
7. Sandip Tiwari, Compound Semiconductor Device Physics, Academic Press (1991), ISBN 0-12-691740-X.

Subject Code	Subject Name	L-T-P	Credit
EC2*112	MEMS and Microsystems and NEMS	**3-0-0**	**3**

Module 1 (6 Hours)

An introduction to Micro sensors and MEMS, Evolution of Micro sensors & MEMS, Micro sensors & MEMS applications

Module 2 (12 Hours)

Microelectronic technologies for MEMS, Micromachining Technology, Surface and Bulk Micromachining, working principle of various MEMS.

Module 3 (12 Hours)

Micro machined Micro sensors: Mechanical, Inertial, Biological, Chemical, Acoustic, Microsystems Technology, Integrated Smart Sensors and MEMS.

Module 4 (12 hours)

Interface Electronics for MEMS, MEMS Simulators, MEMS for RF Applications, Bonding & Packaging of MEMS, Conclusions & Future Trends.

References:

1. Tai-ran Su, MEMS and Microsystems: design and Manufacture, Tata McGraw Hill.
2. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983.
3. S.M. Sze (Ed), VLSI Technology, McGraw Hill, 1988.
4. Julian W. Gardner, V. K. Varadan, Osama O. Awadelkarim, Microsensors, MEMS, and Smart Devices, ISBN: 047186109X - John Wiley and Sons.
5. Gere & Timoshenko, Mechanics of Materials, PWS-KENT, 1990.
6.Gregory T. A. Kovacs, Micromachined Transducers Sourcebook, WGB/McGraw-Hill,2000, ISBN: 0072907223.
7. M. Madou, Fundamentals of Microfabrication, CRC Press, 2002, ISBN: 0849308267
8. M. Elwenspoek & H. Jansen, Silicon micromachining, Cambridge, 1998, ISBN: 052159054
9. S. Senturia, Microsystem Design, Kluwer Academic Publishers, 2001, ISBN: 0792372468
10. S.Sze, Semiconductor Sensors, John Wiley & Sons, 1994 ISBN: 0471546097
Marc Madou, Fundamentals of Microfabrication, CRC Press, 1997.

Subject Code	Subject Name	L-T-P	Credit
EC2*113	Formal Verification of VLSI Circuits	**3-0-0**	**3**

Scope of testing and verification in VLSI design process. Issues in test and verification of complex chips, embedded cores and SOCs.

Fundamentals of VLSI testing. Fault models. Automatic test pattern generation. Design for testability. Scan design. Test interface and boundary scan. System testing and test for SOCs. Iddq testing. Delay fault testing. BIST for testing of logic and memories. Test automation. Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.

Reference:

1. **M. L. Bushnell and V.D. Agrawal, *Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits*, Springer, 2005**
2. H. Fujiwara, *Logic Testing and Design for Testability*, MIT Press, 1985
3. M. Abramovici, M. Breuer, and A. Friedman, *Digital System Testing and Testable Design*, IEEE Press, 1994
4. **M. Huth and M. Ryan, Logic in Computer Science, Cambridge Univ. Press, 2004**
5. **T. Kropf, Introduction to Formal Hardware Verification, Springer Verlag, 2000**
6. Current Literature
7. Class notes

Prerequisite: Knowledge of Digital System Design

Subject Code	Subject Name	L-T-P	Credit
EC2*114	Artificial Intelligence	**3-0-0**	**3**

Overview: foundations, scope, problems, and approaches of AI.

Module 1 (10 Hrs.)
Intelligent agents: reactive, deliberative, goal-driven, utility-driven, and learning agents Artificial Intelligence programming techniques. Problem-solving through Search: forward and backward, state-space, blind, heuristic, problem-reduction, A, A*, AO*, minimax, constraint propagation, neural, stochastic, and evolutionary search algorithms, sample applications.

Module 2 (10 Hrs.)
Knowledge Representation and Reasoning: ontologies, foundations of knowledge representation and reasoning, representing and reasoning about objects, relations, events, actions, time, and

space; predicate logic, situation calculus, description logics, reasoning with defaults, reasoning about knowledge, sample applications.

Module 3 (15 Hrs.)
Planning: planning as search, partial order planning, construction and use of planning graphs. Representing and Reasoning with Uncertain Knowledge: probability, connection to logic, independence, Bayes rule, bayesian networks, probabilistic inference, sample applications.

Module 4 (5 Hrs.)
Decision-Making: basics of utility theory, decision theory, sequential decision problems, elementary game theory, sample applications.

Texts :
1. S. Russell and P. Norvig, Artificial Intelligence: A Modern Approach, 2nd Ed, Prentice Hall, 2003

References :
1. E. Rich and K. Knight, Artificial Intelligence, McGraw Hill, 1991.
2. P. H. Winston and B. K. P. Horn, Lisp, 3rd Ed, Addison-Wesley, 1989.
3. P. Norvig, Paradigms of Artificial Intelligence Programming: Case studies in Common Lisp, Morgan Kauffman, 1991.
4. I. Bratko, Prolog Programming for Artificial Intelligence, 3rd Ed, Addison-Wesley, 2001.

Subject Code	Subject Name	L-T-P	Credit
EC2*115	Semiconductor Power Devices	**3-0-0**	**3**

Module 1 (10 hours)
Avalanche Breakdown voltage of plane and planar pn junctions, Breakdown voltage improvement Techniques.
High injection level effects in pn junctions. Forward voltage drop in high voltage PIN diodes, and its dependence on carrier lifetime.

Module 2 (14 hours)
Bipolar Power Transistor structures and characteristics, Current-gain, Switching operation, second break down and safe operating area, overlay transistor.
Thyristor operation principles, Reverse and forward blocking voltage and forward conduction characteristics. Cathode shorted and Anode shorted Thyristor. di/dt and dv/dt ratings of thyristors, Triacs and GTO.

Module 3 (14 hours)
Power MOSFET structure, I-V characteristics, on resistance, Minimum size chip design for specific drain breakdown voltage, Switching characteristics, Safe operating area, Insulated Gate Transistor (IGT) –Structure, Operation principle, I-V characteristics and turn off transients, Latch up and its prevention.

Module 4 (6 hours)
Power Integrated Circuit Problems and isolati

References:
1. Baliga, B. Jayant, Power Semiconductor Devices, PWS Publishing Co., Boston, 1996
2. Benda, Vitezslav, John Gowar, and Duncan A. Grant, Chichester , Power semiconductor devices: theory and applications, New York Wiley, c 1999
3. Bose, Bimal K, Modern Power Electronics, Evolution, Technology, and Application, IEEE Press, 1992.
4. Ramshaw, Raymond S., Power Electronics Semiconductor Switches, 2nd ed., London: Chapman & Hall (Kluwer)
5.Rashid, Muhammad H., Upper Saddle River, Power Electronics, Circuits, Devices and Applications, 3rd ed., NJ: Pearson Education, 2003.

Subject Code	Subject Name	L-T-P	Credit
EC2*116	Nanoelectronics	**3-0-0**	**3**

Module 1 (8 hours)
Introduction of Nanoscience and Technology,Challenges going to sub-100 nm MOSFETs – Oxide layer thickness, tunnelling, power density, non-uniform dopant concentration, threshold voltage scaling, lithography, hot electron effects, sub-threshold current, velocity saturation, interconnect issues, fundamental limits for MOS operation. High-K gate dielectrics, effects of high-K gate dielectrics on MOSFET performance,

Module 2 (12 hours)
Novel MOS-based devices –Multiple gate MOSFETs, Silicon-on-nothing, Silicon-on-insulator devices, FD SOI, PD SOI, FinFETs, vertical MOSFETs, strained Si devices

Module 3 (6 hours)
Hetero structure based devices –Type I, II and III Heterojunction, Si-Ge heterostructure, hetero structures of III-V and II-VI compounds - resonant tunnelling devices, MODFET/HEMT

Module 4 (8 hours)
Carbon nanotubes based devices –CNFET, characteristics, Spin-based devices –spinFET, characteristics

Module 5 (8 hours)
Quantum structures –quantum wells, quantum wires and quantum dots, Single electron devices – charge quantization, energy quantization, Coulomb blockade, Coulomb staircase, Bloch oscillations

References:
1. Mircea Dragoman and Daniela Dragoman, Nanoelectronics –Principles & devices, Artech House Publishers, 2005.

2. Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2005.

3. Mark Lundstrom and Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation, Springer, 2005.

4. Vladimir V Mitin, Viatcheslav A Kochelap and Michael A Stroscio, Quantum heterostructures, Cambridge University Press, 1999.

5. S.M. Sze (Ed), High speed semiconductor devices, Wiley, 1990.

6. Manijeh Razeghi, Technology of Quantum Devices, Springer, ISBN 978-1-4419-1055-4.

7. H.R. Huff and D.C. Gilmer, High Dielectric Constant Materials for VLSI MOSFET Applications, Springer 2005, ISBN 978-3-540-21081-8 , (Available on NITC intranet in Springer eBook section) 8.B.R. Nag, Physics of Quantum Well Devices, Springer 2002, ISBN 978-0-7923-6576-1, (Available on NITC intranet in Springer eBook section).

Subject Code	Subject Name	L-T-P	Credit
EC2*117	Low Power CMOS VLSI design	**3-0-0**	**3**

Module 1(12 hours)

Review of power dissipation in CMOS Circuits –static and dynamic power dissipation-Leakage sources, input vector dependence, stack effect, leakage reduction using natural and forced stacks, power gating, power gating methodologies, dynamic voltage scaling, forward and reverse body bias, standby techniques, MTCMOS circuits, level shifters, timing and power planning, choosing the high V_{TH} value, MTCMOS circuits using sleep transistors

Module 2 (14 hours)

Supply voltage scaling approaches: parallelism, pipelining, using multiple supply voltage, module level voltage selection, clustered voltage scaling, level converters, multiple supplies inside a block, supply voltage limitations, Optimum supply voltage, multiple device threshold, Technology level –feature size scaling, threshold voltage scaling, Transistor sizing for energy minimization, dynamic supply voltage scaling, dynamic threshold voltage scaling

Module 3 (6 hours)

Switching activity estimation in static and dynamic logic, signal statistics, intersignal correlations, Reducing switching capacitance through transistor sizing, logic and architecture optimization, layout techniques, logic restructuring, input ordering, data representation, resource allocation, reducing glitching through path balancing, clock gating

Module 4 (10 hours)

Behavioral level transforms, algorithm level transforms, architectural transformations, Operation reduction and substitution, logic level optimization and technology mapping,

Energy recovery, design with reversible logic, adiabatic logic, peripheral circuits, Power gating, signal isolation, state retention and restoration, architectural issues for power gating, Dynamic voltage and frequency scaling.

References:

1. Anantha Chandrakasan, Robert Brodersen, Low-power CMOS design, IEEE press, 1998
2. Kaushik Roy, Sharat C. Prasad, Low-power CMOS VLSI circuit design, John Wiley & Sons, 2000.
3. A.Bellamour, M.I.Elmasri, Low power VLSI CMOS circuit design, Kluwer Academic Press, 1995
4. Siva G.Narendran, Anantha Chandrakasan, Leakage in Nanometer CMOS Technologies, Springer, 2005.
5. Mohab Anis, Mohamed Elmasry, Multi-Threshold CMOS Digital Circuits, Kluwer Academic Publishers, 2003.
6. Michael Keating, David Flynn, Robert Aitken, Alan Gibbons and Kaijian Shi, Low power methodology manual, Springer, 2008.

Subject Code	Subject Name	L-T-P	Credit
EC2*118	Mixed Signal RF IC design	**3-0-0**	**3**

Module 1 (9 hours)

CMOS comparators-Introduction to switched capacitor circuits - basic building blocks – operation and analysis –non ideal effects in switched capacitor circuits-switched capacitor integrators - First order filters –switch sharing –biquad filters.

Module 2 (10 hours)

Basic PLL topology, dynamics of simple PLL, Multiplier, EXOR and JK –flipflop phase detectors, lock acquisition, Phase frequency detector, Loop filters, Charge Pump PLLs, non ideal effects in PLLs.

Module 3 (13 hours)

Data converter fundamentals –DC and dynamic specifications –quantization noise –Nyquist rate D/A converters –decoder based converters –binary scaled converters –thermometer code converters –hybrid converters- Nyquist rate A/D converters-Successive approximation, Flash, interpolating, Folding, Pipelined, Time-interleaved converters

Module 4 (10 hours)

Oversampling converters, Noise shaping modulators, Decimating filters and interpolating filters, Higher **order** modulators, Delta Sigma modulators with multibit quantizers- Delta Sigma D/A

References:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, Tata-Mc GrawHill, 2002.
2. Rudy van de Plassche, CMOS integrated Analog- to Digital and Digital to- Analog converters, Kluwer academic publishers,2003.
3. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.
4. Roland E.Best, Phase Locked Loops, McGraw Hill,2007.
5. Richard Schreier, Understanding Delta-Sigma Data Converters, Wiley Interscience, 2005.

6. R.Jacob Baker, CMOS Mixed-signal Circuit Design, Wiley Student Edition, Wiley Interscience, 2009.

Subject Code	Subject Name	L-T-P	Credit
EC2*119	CMOS RF circuit design	**3-0-0**	**3**

Module 1 (12 hours)

Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers –Transmission lines Classical two-port noise theory, noise models for active and passive components, Noise figure, Friis equation, Nonlinearity and cascaded stages, Sensitivity and dynamic range, Passive impedance transformation.

Module 2 (12 hours)

High frequency amplifier design –zeros as bandwidth enhancers, shunt-series amplifier, fT doublers, neutralization and unilateralization Low noise amplifier design –LNA topologies, impedance matching, power constrained noise optimization, linearity and large signal performance, noise canceling LNAs, Constant gm biasing, current reusing technique.

Module 3 (10 hours)

Mixers –multiplier-based mixers, subsampling mixers, diode-ring mixers

RF power amplifiers –Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations.

Module 4 (8 hours)

Oscillators & synthesizers –describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers –phase noise considerations.

References:

1. Thomas H. Lee, Cambridge, The Design of CMOS Radio-Frequency Integrated Circuits, UK: Cambridge University Press, 2004.

2. Behzad Razavi, RF Microelectronics, Prentice Hall, 1998.

3. A.A. Abidi, P.R. Gray, and R.G. Meyer, eds. Integrated Circuits for Wireless Communications, New York: IEEE Press, 1999.

4. Bosco Leung and Charles G. Sodini, VLSI for wireless communication, Second Impression, Pearson, 2009.

Subject Code	Subject Name	L-T-P	Credit
EC2*120	III-V semiconductors and High Speed electronic Devices	**3-0-0**	**3**

Module 1 (6 hours)

Wave Mechanics and the Schrödinger Equation, Free Particles, Bound Particles: Quantum Well, Charge and Current Densities, operators and current Densities, Expectation Value, Density of states. Electron and Phonons in Cryatals, Heterostructure, Quantum Well and Low dimensional system, Tunnelling Transport, Schrödinger Equation in Electric and Magnetic field, Scattering, 2DEG.

Module 2 (10 hours)

Important parameters governing the high speed performance of devices and circuits: Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature; important parameters governing the high power performance of devices and circuits: Break down voltage, resistances, device geometries, doping concentration and temperature

Module3 (5 hours)

Materials properties:

Merits of III –V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs, SiC, GaN etc.), different SiC structures, silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices,

Module 4 (8 hours)

Metal semiconductor contacts and Metal Insulator Semiconductor and MOS devices: Native oxides of Compound semiconductors for MOS devices and the interface state density related issues. Metal semiconductor contacts, Schottky barrier diode, Metal semiconductor Field Effect Transistors (MESFETs): Pinch off voltage and threshold voltage of MESFETs. D.C. characteristics and analysis of drain current. Velocity overshoot effects and the related advantages of GaAs, InP and GaN based devices for high speed operation. Sub threshold characteristics, short channel effects and the performance of scaled down devices.

Module5 (12 hours)

High Electron Mobility Transistors (HEMT): Hetero-junction devices. The generic Modulation Doped FET(MODFET) structure for high electron mobility realization. Principle of operation and the unique features of HEMT, InGaAs/InP HEMT structures: Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high speed applications. GaAs and InP based HBT device structure and the surface passivation for stable high gain high frequency performance. SiGe HBTs and the concept of strained layer devices; High Frequency resonant – tunneling devices, Resonant-tunneling hot electron transistors.

Reference:

1. C.Y. Chang, F. Kai, GaAs High-Speed Devices: Physics, Technology and Circuit Applications Wiley

2. Cheng T. Wang, Ed., Introduction to Semiconductor Technology: GaAs and Related Compounds, John Wiley & Sons,

3. David K. Ferry, Ed., Gallium Arsenide Technology, Howard W. Sams & Co., 1985

4. Avishay Katz, Indium Phosphide and Related materials: Processing, Technology and Devices, Artech House, 1992.

5. S.M. Sze, High Speed Semiconductor Devices, Wiley (1990) ISBN 0-471-62307-5

6. Ralph E. Williams, Modern GaAs Processing Methods, Artech (1990), ISBN 0-89006-343-5,
7. Sandip Tiwari, Compound Semiconductor Device Physics, Academic Press (1991), ISBN 0-12-691740-X
8. G.A. Armstrong, C.K. Maiti, TCAD for Si, SiGe and GaAs Integrated Circuits, The Institution of Engineering and Technology, London, United Kingdom, 2007,ISBN 978-0-86341-743-6.
9. John H. Davies, " The Physics of Low-Dimensional Semiconductors an Introduction", Cambridge University Press, 1998.

Subject Code	Subject Name	L-T-P	Credit
EC2*121	Biomedical Instrumentation	**3-0-0**	**3**

Course Objectives: The objective of this course is to introduce student to basic biomedical engineering technology and introduce different biological signals, their acquisition, measurements and applications.

Introduction of Bio-medical Instrumentation: 6L

Human body systems, cell, tissue, muscle, organ; excitable cells, resting and active potentials, electrode theory, biopotential electrodes, biopotential amplifiers.

Nervous System: 8L

Neurons, types of neurons, factors affecting nerve conduction, EMG signal acquisition and processing, application of EMG signal. CNS, brain and their function, Electroencephalography, signal characteristics, electrode placement, acquisition and applications.

Cardiopulmonary System: 10L

Heart and its functioning, electrocardiography, electrode positions, ECG signal characteristics, signal acquisition, processing, analysis and applications of ECG signal, heart sounds. their characteristics and acquisition, cardiac output, blood, blood pressure, blood flow, pulse oxymetry, respiration organs and their functions, respiration measurements.

Therapeutic and Safety: 5L

Pacemakers, defibrillators, ventilators, heart-lung machines, hemo-dialysis, lithotripsy, applications of LASERs, Electric current, voltage and their effects on human body, safety norms, earthing, first aid techniques, Cardio-pulmonary resuscitation.

Medical Imaging principles and applications: 7L

X-Ray, CAT, MRI, fMRI, PET and SPECT, Ultrasound, thermography, medical image processing applications.

Text Books:

1. L. Cromwell, F. J. Weibell, and L. A. Pfeiffer, **Biomedical Instrumentation and Measurements**, Pearson Education, Delhi,
2. J. J. Carr and J. M. Brown, **Introduction to Biomedical Equipment Technology**, Pearson Education, Delhi,
3. S. Chatterjee, **Biomedical Instrumentation Systems**, Cengage learning 2011

Reference Books:

4. L.A. Geddes and L.E. Baker, **Principles of Applied Biomedical Instrumentation**, John Wiley & Sons, Inc,

Subject Code	Subject Name	L-T-P	Credit
EC2*122	Advanced communication systems	**3-0-0**	**3**

Pre-requisites: Digital Communication, Wireless Communication.

MODULE – I:

Review of Digital Communication system: Source coder: PCM-DPCM-DM, Channel coder. Digital modulation techniques: ASK-FSK-PSK-MSK-GMSK-QAM. Spread spectrum modulation techniques: DSSS, FHSS. Design of transmitter and receiver for digital signal transmission and reception. Design trade off.

MODULE – II:

Multiple Access Techniques – TDMA, FDMA, CDMA. Concept of OFDM, OFDM transmitter and receiver design. OFDM Issues – PAPR; Frequency and Timing Offset Issues. Introduction to MIMO, MIMO Receiver Design: Zero Forcing and MMSE Receiver; MIMO channel decomposition, Optimal Power Allocation strategy; MIMO Spatial Multiplexing – VBLAST; MIMO Diversity – Alamouti Code, OSTBC.

MODULE – III:

4^{th} and 5^{th} generation wireless communication system design. Concept of cognitive radio (CR), Transceiver design for CR. System design for wireless Adhoc network: Bluetooth, Zigbbe, UWB. Antennas for 4^{th} and 5^{th} generation mobile communication, smart antenna, MIMO antenna.

Text Books:

1. B. Sklar and P.K. Ray, Digital Communication: Fundamentals and Applications, Pearson Education.
2. Rapport Thoedore S., Wireless Communications, Principles and Practice, PHI,

Reference:

1. Andrea Goldsmith, Wireless Communications, Cambridge University Press.
2. G. L. Stuber, Principles of mobile communications, 2nd Ed., Springer.
3. MIMO Wireless Communications " Ezio Biglieri" Cambridge University Press.

Subject Code	Subject Name	L-T-P	Credit
EC2*123	Computer Architecture	**3-0-0**	**3**

Module 1

Fundamentals: Technology trend -Performance measurement –Comparing and summarizing performance- quantitative principles of computer design –Amdahl's law-Case studies. Principles of processor performance - Processor performance optimization- Performance evaluation methods

Module 2

Features of advanced Intel processors**:** Enhancements of 80386 and Pentium -Hardware Features, PVAM,-Memory management unit-Virtual Memory and concepts of cache -32 bit programming

Module 3

Instruction and thread level parallelism: Instruction level parallelism and concepts - - Limitations of ILP- Multiprocessor and thread level parallelism- Pipelining: Issues and solutions- Instruction flow techniques -Program control flow and control dependences

Module 4

Superscalar and multi core techniques: General principles of superscalar architecture - -Basics ,Pipelining**,** The in-order front end, The out-of-order core, The reorder buffer, Memory subsystem- Multi core processing – facts and figures - Virtualization –concepts

References:

1. John Shen and Mikko H Lipasti, Modern Processor Design: Fundamentals of Superscalar Processors, McGraw Hill Publishers , 2005
2. LylaB.Das, The x86 Microprocessors, Architecture, Programming and Interfacing Pearson Education, 2010
3. Hennessy J. L. & Patterson D. A., Computer Architecture: A Quantitative approach, 4/e, Elsevier Publications, 2007.
4. Patterson D. A. & Hennessy J. L., Computer Organisation and Design: The Hardware/ Software Interface, 3/e, Elsevier Publishers, 2007
5. JurijSilc, BorutRobic, ThUngerer: Processor Architecture: From Dataflow to Superscalar and Beyond. Springer-Verlag, June 1999

Subject Code	Subject Name	L-T-P	Credit
EC2*124	VLSI Signal Processing	**3-0-0**	**3**

Module 1(8 hours): Pipelining and Parallel Processing: introduction, pipelining of FIR Digital filters Parallel processing. Pipelining and parallel processing for low power.

Module 2(10 hours): Retiming: Introduction, Definition and properties, Solving system of inequalities, retiming techniques. Unfolding, Introduction An algorithms for unfolding, Properties of unfolding, Critical path, unfolding and retiming Application of unfolding.

Module 3(8 hours): Folding: Introduction Folding Transformation, Register Minimization Techniques, Register minimization in folded architectures Folding if Multirate systems.

Module 4(8 hours): Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR systolic Arrays, Selection of scheduling vector, Matrix Multiplication and 2D systolic array Design, Systolic design for space representations containing Delays.

Module 5(8 hours): Fast Convolution: Introduction, Cook, Toom algorithm, Winogard algorithm, iterated convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

References

1. Rafel C. Gonzalez and Richard E. Woods "Digital image processing", Addition-wisely
2. Anil K.Jain "Fundamental of digital image processing" prentice Hall 1995.
3. Rosenfeld A.C. Kak, Digital picture processing-academic press inc 1976.
4. Hall E.L. computer image processing and recognition academic press inc 1979.
5. Huang T.S. "Picture processing and digital filtering" Springer Verlag Berlin Heidelberg.

Subject Code	Subject Name	L-T-P	Credit
EC2*125	Semiconductor Materials and Device characterization	**3-0-0**	**3**

Module I (10 hrs): Structural Characterizations
High Resolution X-Ray Diffraction stydy (HRXRD), Field Emission Scanning Electron Microscopy analysis (FESEM), High resolution transmission Electron Microscopy analysis(HRTEM), Scanning Probe Microscopic Analysis (SPM)
Module II (7 hrs): Optical Characterizations
Ellipsometry, Photoluminescence, UV-Visible spectroscopy, FTIR, Raman spectroscopy, X-Ray Photolectron spectroscopy analysis (XPS)
Module III (15 hrs): Electrical Characterization
Resistivity (r): Four point probe, Spreading Resistance, Microwave and RF absorption methods.
Carrier density (n, p): Hall Effect, I-V, C-V, Capacitance-Voltage (C-V), Optical absorption,
Carrier mobility (m): Resistivity and Hall Effect, Magnetoresistance
Module IV (8hrs): Chemical and Physical Characterization, Auger Electron Spectroscopy(AES), Secondary Ion Mass Spectroscopy(SIMS), Rutherford Back Scattering(RBS).
Reference:

1. Dieter K. Schroder, "Semiconductor Material and Device Characterization" John Wiley & Sons, INC, Second Edition.
2. Ayers J. E "Heteroepitaxy of Semiconductors Theory, Growth, and Characterization" (CRC Press, Taylor & Francis Group, New York, 2007),
3. D. Keith Bowen and Brain K. Tanner, "High Resolution X-ray Diffractometry and Topography" Tailor & Francis.

Subject Code	Subject Name	L-T-P	Credit
EC2*126	VLSI Technology and Processing	**3-0-0**	**3**

Module 1 (6 hours)

Material properties, crystal structure, lattice, basis, planes, directions, angle between different planes, defects, characterization of material based on band diagram and bonding, conductivity, resistivity, sheet resistance, phase diagram and solid solubility, Crystal growth techniques, Heterostructures, wafer cleaning, Epitaxy, Clean room and safety requirements

Module 2 (15 hours)

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films, Deal-Grove model and Improvements in Deal-Grove method for thin and ultra thin oxide layers, thickness characterization methods, multi dimension oxidation modeling

Diffusion and Ion Implantation: Diffusion process, Solid state diffusion modeling, various doping techniques, Ion implantation, modeling of Ion implantation, statistics of ion implantation, damage annealing, thermal budget, rapid thermal annealing, spike anneal, advanced annealing methods, Implant characterization SIMS, spreading resistance method

Module 3 (15 hours)

Deposition & Growth**:** Homogeneous and Heterogeneous growth**,**Various deposition techniques CVD, PVD, evaporation, sputtering, spin coating, LPCVD, epitaxy, MBE, ALCVD, Growth of High k and low k dielectrics

Etch and Cleaning**:** materials used in cleaning, various cleaning methods, Wet etch, Dry etch, Plasma etching, RIE etching, etch selectivity/selective etch

Photolithography: Positive photo resist, negative photo resist, comparison of photo resists, components of a resist, light sources, exposure, Resolution, Depth of Focus, Numerical Aperture (NA), sensitivity, contrast, need for different light sources, masks, Contact, proximity and projection lithography, step and scan, optical proximity correction, develop(development of resist), Next generation technologies: Immersion lithography, Phase shift mask, EUV lithography, X-ray lithography, e-beam lithography, ion lithography, SCALPEL

Module 4 (6 hours)

Planarization Techniques: Need for planarization, Chemical Mechanical Polishing. Metallization and Interconnects: Copper damascene process, Metal interconnects; Multi-level metallization schemes, Process integration: NMOS, CMOS and Bipolar process.

Reference:

1. M. Deal and P.Griffin, Silicon VLSI Technology, James Plummer, Prentice Hall Electronics, 2010.

2. Stephen Campbell, The Science and Engineering of Microelectronics Oxford University Press, 1996. 3. S.M. Sze, VLSI Technology, 2nd Edition, McGraw Hill, 1988. 4. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983. 5. C.Y. Chang and S.M.Sze , ULSI Technology, McGraw Hill Companies Inc, 1996.

3. Ayers J. E Heteroepitaxy of Semiconductors Theory, Growth, and Characterization (CRC Press, Taylor & Francis Group, New York, 2007)

4. S. M.Sze, " VLSI Technology" McGraw-Hill, 1983.

5. S. K. Gandhi, "VLSI fabrication principles", 1983.

Subject Code	Subject Name	L-T-P	Credit
EC2*127	Introduction to VLSI Design	**3-0-0**	**3**

Module 1 (11 hours)

Introduction MOSFET, threshold voltage, current, Channel length modulation, body bias effect and short channel effects, MOS switch, MOSFET capacitances, MOSFET models for calculation-Transistors and Layout, CMOS layout elements, parasitics, wires and vias-design rules-layout design SPICE simulation of MOSFET I-V characteristics and parameter extraction

Module 2 (10 hours)

CMOS inverter, static characteristics, noise margin, effect of process variation, supply scaling, dynamic characteristics, inverter design for a given VTC and speed, effect of input rise time and fall time, static and dynamic power dissipation, energy & power delay product, sizing chain of inverters, latch up effect-Simulation of static and dynamic characteristics, layout, post layout simulation

Module 3 (13 hours)

Static CMOS design, Complementary CMOS, static properties, propagation delay, Elmore delay model, power consumption, low power design techniques, logical effort for transistor sizing, ratioed logic, pseudo NMOS inverter, DCVSL, PTL, DPTL & Transmission gate logic, dynamic CMOS design, speed and power considerations, Domino logic and its derivatives, C2MOS, TSPC registers, NORA CMOS –Course project

Module 4 (8 hours)

Circuit design considerations of Arithmetic circuits, shifter, CMOS memory design - SRAM and DRAM, BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic

References:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, , MGH, Third Ed., 2003

2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective,Prentice Hall, Second Edition, 2005

3. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, Third Edition, McGraw-Hill, 2004

4. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation, Wiley-IEEE Press, 2007

5. Christopher Saint and Judy Saint, IC layout basics: A practical guide, McGraw-Hill Professional, 2001

Subject Code	Subject Name	L-T-P	Credit
EC2*128	Analytical Techniques for VLSI	**3-0-0**	**3**

Historical Perspective of VLSI**,** CMOS VLSI Design for Power and Speed consideration, Logical Efforts: Designing Fast CMOS Circuits; Datapath Design, Interconnect aware design, Hardware Description Languages for VLSI Design, FSM Controller/Datapath and Processor Design, VLSI Design Automation, and VLSI Design Test and Verification.

Subject Code	Subject Name	L-T-P	Credit
EC2*129	Signal Processing Technique	**3-0-0**	**3**

Module 1: Review of random variables:

Distribution and density functions, moments, independent, uncorrelated and orthogonal random variables; Vector-space representation of Random variables, Schwarz Inequality Orthogonalit principle in estimation, Central Limit theorem, Random processes, wide-sense stationary processes, autocorrelation and autocovariance functions, Spectral representation of random signals, Linear System with random input.

Module 2: Parameter Estimation Theory:
Principle of estimation and applications, Properties of estimates, the methods of maximum likelihood and its properties ;Baysean estimation : Mean square error and MMSE, Mean Absolute error.

Module 3: Estimation of signal in presence of white Gaussian Noise:

Linear Minimum Mean-Square Error (LMMSE) Filtering: FIR Wiener filter, Causal IIR Wiener filter, Noncausal IIR Wiener filter, Linear Prediction of Signals, Forward and Backward Predictions, Levinson Durbin Algorithm.

Module 4: Adaptive Filtering:
Principle and Application, Steepest Descent Algorithm Convergence characteristics; LMS algorithm, convergence, excess mean square error, Leaky LMS
algorithm;Application of Adaptive filters; RLS algorithm, derivation, Matrix inversion Lemma, Intialization, tracking of nonstationarity.

References:

1.M. Hays: Statistical Digital Signal Processing and Modelling, John Willey and Sons, 1996.
2. M.D. Srinath, P.K. Rajasekaran and R. Viswanathan: Statistical Signal Processing with Applications, PHI, 1996.
3. Simon Haykin: Adaptive Filter Theory, Prentice Hall, 1996.

4. D.G. Manolakis, V.K. Ingle and S.M. Kogon: Statistical and AdaptiveSignal Processing, McGraw Hill, 2000.
5. S. M. Kay: Modern Spectral Estimation, Prentice Hall, 1987

Subject Code	Subject Name	L-T-P	Credit
EC2*130	Embedded System	**3-0-0**	**3**

Module 1(10 hours):
Introduction to Embedded systems : Embedded system examples, Parts of Embedded System- Processor, Power supply, clock, memory interface, interrupt, I/O ports, Buffers, Programmable Devices, ASIC,etc. interfacing with memory and I/O devices. Memory Technologies – EPROM, Flash, OTP, SRAM,DRAM, SDRAM etc.

Module 2 (8 hours):
Embedded System Design: Embedded System product Development Life cycle (EDLC), Hardware development cycles- Specifications, Component selection, Schematic Design, PCB layout, fabrication and assembly. Product enclosure Design and Development.

Embedded System Development Environment – IDE, Cross compilation, Simulators/Emulators, Hardware Debugging. Hardware testing methods like Boundary Scan, In Circuit Testing (ICT) etc. Bus architectures like I2C, SPI, AMBA, CAN etc.

Module 3 (12 hours) Operating Systems:
Concept of firmware, Operating system basics, Real Time Operating systems, Tasks, Processes and Threads, Multiprocessing and Multitasking, Task scheduling, Task communication and synchronisation, Device Drivers.

Module 4 (12 hours)
System Design Examples : System design using ARM/PSoC/MSP430 processor

Reference:
1. Shibu K.V.: Introduction to Embedded Systems, Tata McGraw Hill, 2009
2. Tim Wilmshurst: An introduction to the design of small-scale embedded systems, Palgrave, 2001.
3. Device data sheets of ARM/PSoC/MSP430
4. Web Resources

Subject Code	Subject Name	L-T-P	Credit
EC2*131	Internet of Things	**3-0-0**	**3**

Module 1
Wireless Technologies for IoT: Wireless Ad-hoc network protocols standards- WLAN, Zigbee, Bluetooth, UWB- applications. Bluetooth Low Energy (BLE). Wireless Sensors for IoT- Synchronization and Localization, Reconfigurable Sensor Networks
Module 2

Embedded systems for IoT- Overview, characteristics and architecture, Processor basics and System-On-Chip. Sensor based applications through embedded system - Home control, Building automation, Industrial automation, Medical applications.

Module 3

Characteristics, Architectural overview and Functional blocks of IoT. Physical and Logical Design of IoT. IoT architecture outlines and standards. M2M and IoT Technology Fundamentals and differences, Local and wide area networking, Communication models and APIs.

References:

1. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", 1 st Edition, Academic Press, 2014.
2. Peter Waher, "Learning Internet of Things", PACKT publishing, Birmingham – Mumbai
3. Bernd Scholz-Reiter, Florian Michahelles, "Architecting the Internet of Things", ISBN 978-3-642-19156-5 e-ISBN 978-3-642-19157-2, Springer
4. Daniel Minoli, "Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications", ISBN: 978-1-118- 47347-4, Willy Publications

Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-on Approach)", 1st Edition, VPT, 2014

Subject Code	Subject Name	L-T-P	Credit
EC2*132	Modeling of Digital Systems	**3-0-0**	**3**

Module 1

Introduction to HDL based Digital Design: – Basic VHDL terminology – basic language elements – Data objectsand types – Behaviouralmodelling – Process constructs – Complex signal assignments – Dataflow modelling –delay models – Structural modelling – resolving signal values

Module 2

Advanced VHDL features: Generics and Configurations – Subprograms and Overloading – Packages andLibraries – Advanced features – simulation semantics – modelling examples – state machine modelling usingVHDL- review of FPGA architectures and design using FPGA. Practical design exercises on VHDL simulator/synthesizer

Module 3

Digital System Testing: Fault models – fault equivalence – fault location fault dominance – single and multiplestuck faults – Testing for single stuck faults – Algorithms – random test generation – Testing for bridging faults

Module 4

Design for Testability: Ad-hoc design for testability techniques – Classical scan designs – Boundaryscanstandards – Built-in-self-test – Test pattern generation – BIST architecture examples.

Reference:

1. J. Bhasker; A VHDL Synthesis Primer, B.S. Publications 2001

2. Kenneth L Short, VHDL for Engineers, Pearson Education ,2006
3. MironAbramovici, et. al. Digital System Testing and Testable Design, Jaico Publishing, 2001
4. Charles H. Roth Jr; Digital System Design Using VHDL, Thomson Education,2005

Subject Code	Subject Name	L-T-P	Credit
EC2*133	Research Methodology	**3-0-0**	**3**